600 mA, 6 MHz, Synchronous Step-Down, DC-to-DC Converter

ADP2121

FEATURES

Peak efficiency: 92%
Operating frequency: 6 MHz
Typical quiescent current in auto mode: 36 µA
Fixed output voltage: 1.82 V
Maximum guaranteed load current: 600 mA at V_{IN} ≥ 2.7 V
Input voltage: 2.3 V to 5.5 V
Typical shutdown supply current: 0.3 µA
Automatic power-saving mode
Compatible with tiny multilayer inductors
Internal synchronous rectifier
Internal compensation
Internal soft start
Output to ground short circuit protection
Cycle by cycle current-limit protection
Enable/shutdown logic input
Undervoltage lockout
Thermal shutdown protection
Ultrasmall 6-ball, 0.4 mm pitch, 1.17 mm² WLCSP

APPLICATIONS

Mobile phones
Digital cameras
Digital audio
Portable equipment

GENERAL DESCRIPTION

The ADP2121 is a high frequency, low quiescent current, step-down, dc-to-dc converter optimized for portable applications in which board area and battery life are critical constraints. Fixed frequency operation at 6 MHz enables the use of tiny ceramic inductors and capacitors. Additionally, the synchronous rectification improves efficiency and results in fewer external components. At high load currents, the device uses a voltage regulating pulse-width modulation (PWM) mode that maintains a constant frequency with excellent stability and transient response. In forced PWM mode, the converter continues operating in PWM for light loads. At light load conditions in auto mode, the ADP2121 can automatically enter a power saving mode that uses pulse-frequency modulation (PFM) to reduce the effective switching frequency and ensure the longest battery life in portable applications. During logic controlled shutdown (EN ≤ 0.4 V), the input is disconnected from the output and draws less than 0.3 µA current (typical) from the source.

The ADP2121 has an input voltage range of 2.3 V to 5.5 V allowing the use of a single Li+/Li– polymer cell, 3-cell alkaline or Ni-MH cell, and other standard power sources. The converter is internally compensated to minimize external components, and the 1.82 V fixed output voltage can source up to 600 mA. Other key features such as cycle-by-cycle peak current limit, soft start, undervoltage lockout (UVLO), output-to-ground short circuit protection, and thermal shutdown provide protection for internal and external circuit components.

TYPICAL APPLICATION CIRCUIT

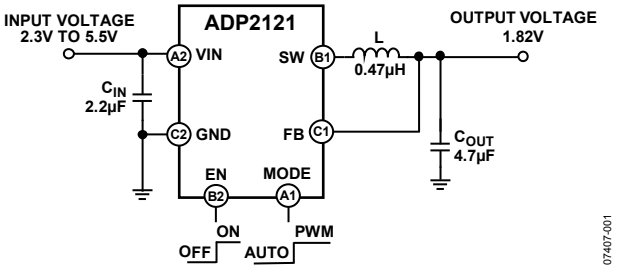

Figure 1. Circuit Configuration of ADP2121

TYPICAL PERFORMANCE

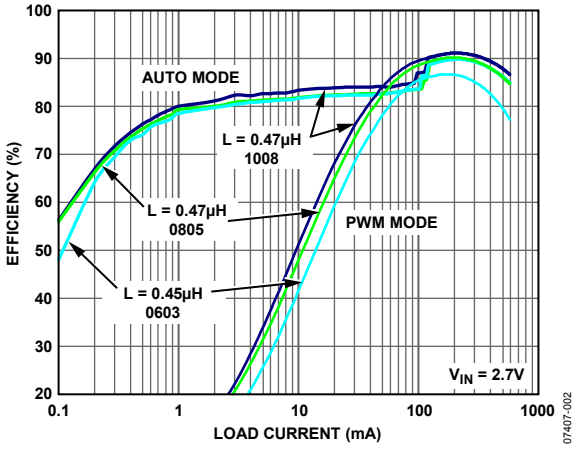

Figure 2. Efficiency vs. Load Current for Various Inductors

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

4/09—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = EN = 3.6 V, typical values are at T_A = 25°C, and minimum/maximum limits guaranteed for T_J = −40°C to +125°C,[1] unless otherwise noted.

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
SUPPLY					
Input Voltage Range		2.3		5.5	V
Quiescent Current	V_{IN} = 3.6 V, auto mode, no load, not switching, T_A = −40°C to 85°C		36	56	µA
	V_{IN} = 3.6 V, PWM mode, no load		10		mA
Shutdown Current	V_{EN} = 0 V, T_A = −40°C to 85°C		0.3	1	µA
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout Threshold	V_{IN} rising		2.1	2.3	V
	V_{IN} falling	1.57	2.0		V
OUTPUT					
Continuous Output Current[2]	V_{IN} = 2.3 V	300			mA
	V_{IN} = 2.5 V	500			mA
	V_{IN} = 2.7 V to 5.5 V	600			mA
Output Accuracy[3]	Auto mode, V_{IN} = 3.6 V, T_A = 25°C, no load, V_{NOM} = 1.82 V	−3		+3	%
	PWM mode, V_{IN} = 2.5 V to 4.5 V, no load, V_{NOM} = 1.82 V	−3		+3	%
Load Regulation	PWM mode, I_{LOAD} = 1 mA to 600 mA		−0.07		%/A
Feedback Bias Current	V_{FB} = 1.82		3.8	8	µA
SWITCHING CHARACTERISTICS					
SW On Resistance (R_{DSon})	P-channel switch		220	440	mΩ
	N-channel synchronous rectifier		260	550	mΩ
SW Leakage Current	V_{IN} = 5.5 V, V_{SW} = 0 V and 5.5 V			5	µA
SW Current Limit	P-channel switch, open loop, V_{IN} = 3.6 V, T_A = −40°C to 125°C	790	1000	1222	mA
	P-channel switch, open loop, V_{IN} = 3.6 V, T_A = −40°C to 85°C	828	1000	1222	mA
Oscillator Frequency		5.36	6	6.64	MHz
EN/MODE INPUT LOGIC	V_{IN} = 2.3 V to 5.5 V				
High Threshold Voltage		1.2			V
Low Threshold Voltage				0.4	V
Leakage Current	V_{IN} = V_{EN} = V_{MODE} = 5.5 V		0.01	1	µA
SOFT START	Time from EN ≥ 1.2 V to stable V_{OUT}				
Soft Start Period[4]	V_{IN} = 3.6 V, R_{LOAD} = 5.1 Ω		275	310	µs
SHORT CIRCUIT THRESHOLD			1.24		V
THERMAL SHUTDOWN					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC); typical values are at T_A = 25°C.
[2] Guaranteed by design. The maximum output current guarantee for 2.3 V to 2.5 V increases linearly from 300 mA to 500 mA. The maximum output current guarantee for 2.5 V to 2.7 V increases linearly from 500 mA to 600 mA. Above 2.7 V, the maximum output current guarantee is 600 mA.
[3] Transients not included in voltage accuracy specifications. For PFM mode, the VOUT accuracy specification is for the upper point of the ripple.
[4] Typical value characterized on bench. Maximum specification guaranteed by design. C_{IN} = 2.2 µF (GRM155R60J225M), L = 0.47 µH (LQM2HPNR47MG0L), C_{OUT} = 4.7 µF (GRM155R60J475ME87D).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +6 V
EN, MODE to GND	−0.3 V to VIN
FB, SW to GND	−0.3 V to VIN + 0.2 V
Operating Ambient Temperature Range (@ I_{LOAD} = 600 mA)	−40°C to +85°C
Operating Junction Temperature Range	−40°C to + 125°C
Storage Temperature	−45°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD (Electrostatic Discharge)	
Human Body Model	±4 kV
Charged Device Model	±1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP2121 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 2- and 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required.

The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. Refer to JEDEC JESD51-9 for detailed information about board construction.

THERMAL RESISTANCE

The junction-to-ambient thermal resistance of the system (θ_{JA}) is specified for worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
6-Ball WLCSP		
2-Layer Board	198	°C/W
4-Layer Board	105	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

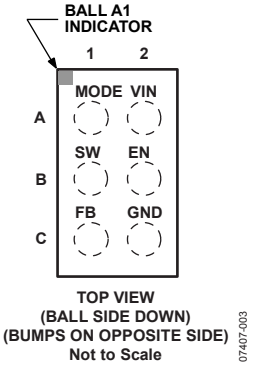

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	MODE	Mode Select. This pin toggles between auto mode (PFM and PWM switching) and PWM mode. Set MODE low to allow the part to operate in auto mode. Pull MODE high to force the part to operate in PWM mode. The voltage applied to MODE can never be higher than the voltage applied to VIN. Do not leave this pin floating.
B1	SW	Switch Node.
C1	FB	Feedback Divider Input. Connect the output capacitor from FB to GND as close as possible to the ADP2121 to set the output voltage ripple and to complete the control loop.
A2	VIN	Power Supply Input. Connect the input capacitor from VIN to GND as close as possible to the ADP2121.
B2	EN	Enable. Pull this pin high to enable the part. Set this pin low to disable the part. Do not leave this pin floating.
C2	GND	Ground Pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, L = 0.47 µH (1800 mA, 1008, LQM2HPNR47MG0L), C_{IN} = 2.2 µF (6.3 V, 0402, X5R, GRM155R60J225M), C_{OUT} = 4.7 µF (6.3 V, 0402, X5R, GRM155R60J475ME87D), EN = V_{IN}, and T_A = 25°C, unless otherwise noted.

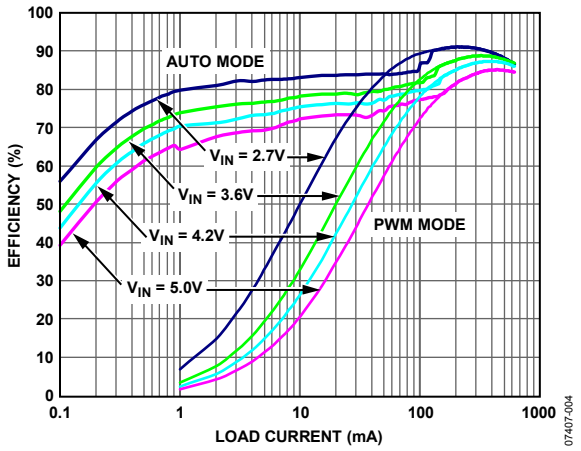

Figure 4. Efficiency vs. Load Current

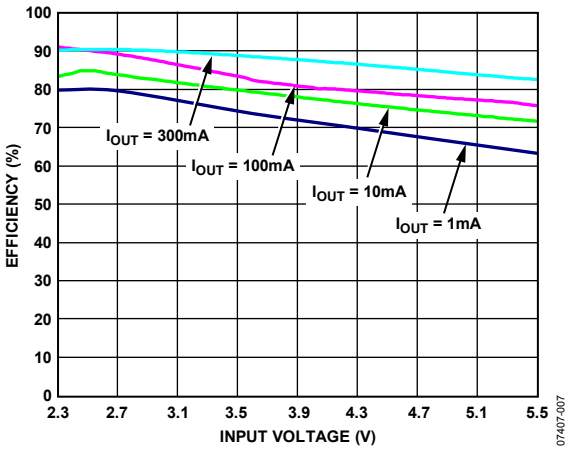

Figure 7. Efficiency vs. Input Voltage (Auto Mode)

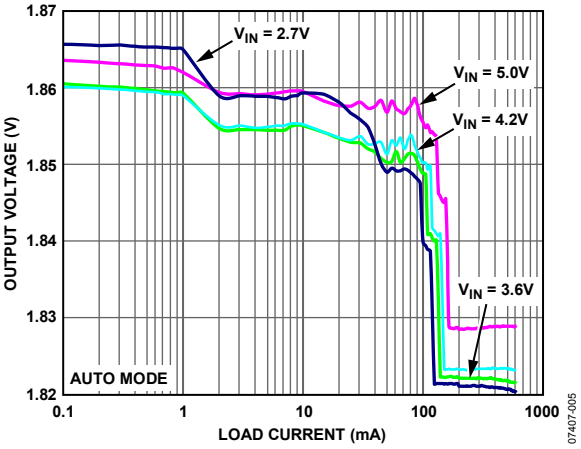

Figure 5. Output Voltage Accuracy (Auto Mode)

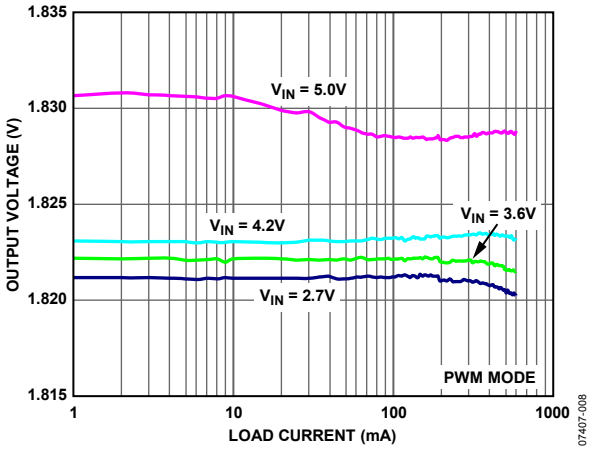

Figure 8. Output Voltage Accuracy (PWM Mode)

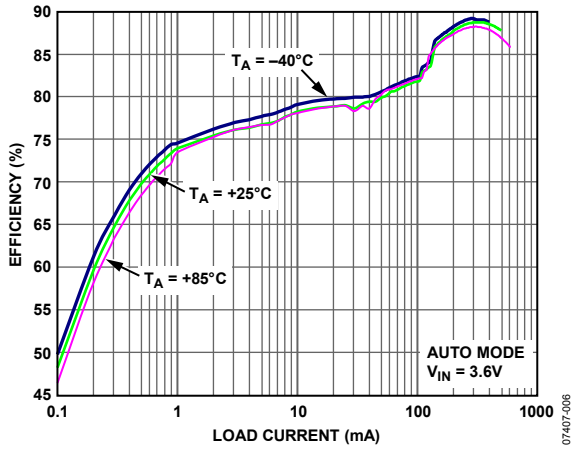

Figure 6. Efficiency vs. Load Current Over Temperature

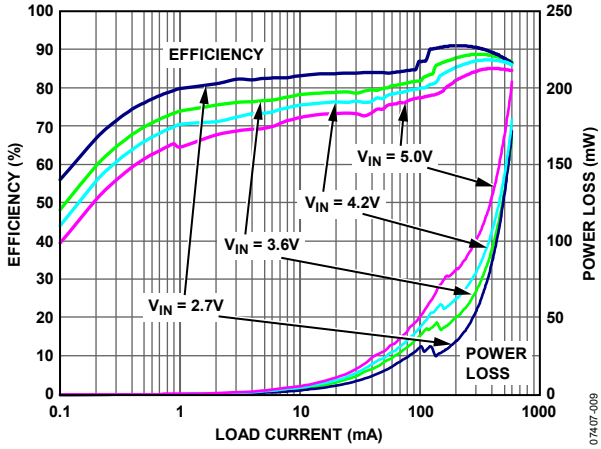

Figure 9. Efficiency and Power Loss vs. Load Current (Auto Mode)

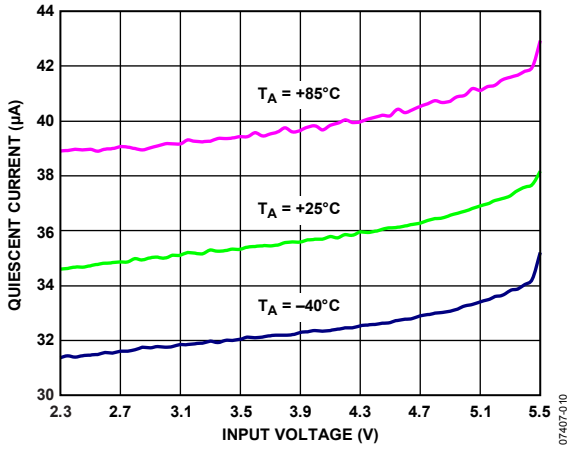

Figure 10. Auto Mode Quiescent Current (Nonswitching, No Load)

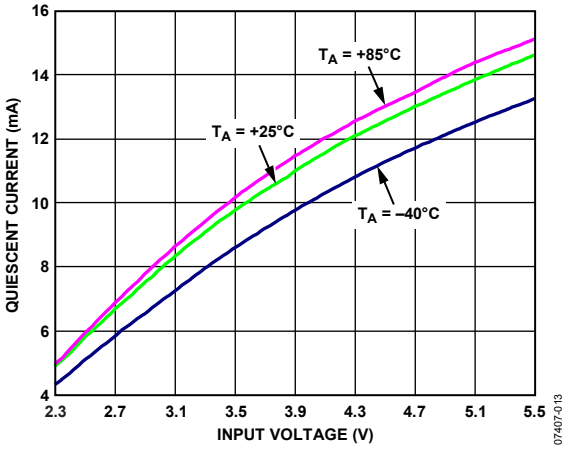

Figure 13. PWM Mode Quiescent Current (Switching, No Load)

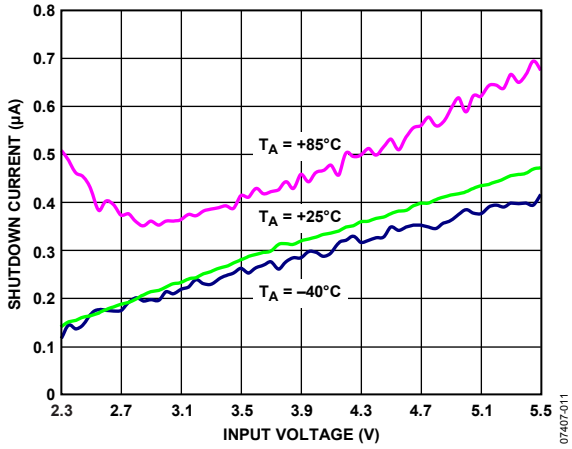

Figure 11. Shutdown Current vs. Input Voltage Over Temperature

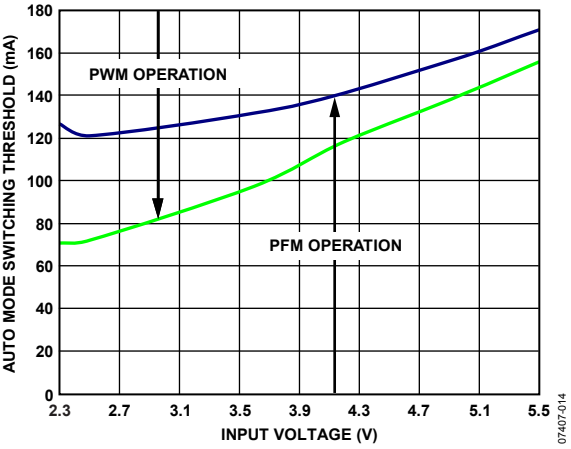

Figure 14. Auto Mode Switching Threshold vs. Input Voltage

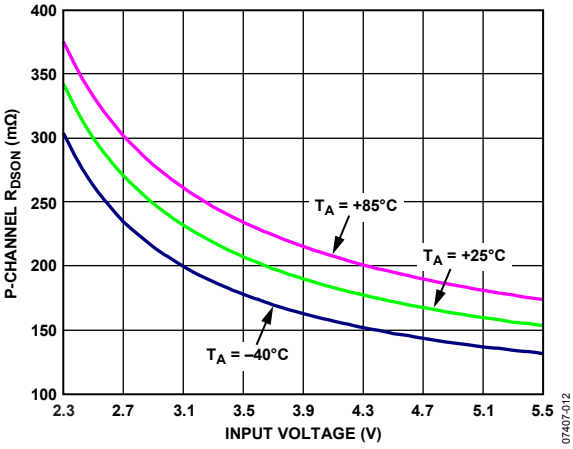

Figure 12. P-Channel Drain-Source On Resistance

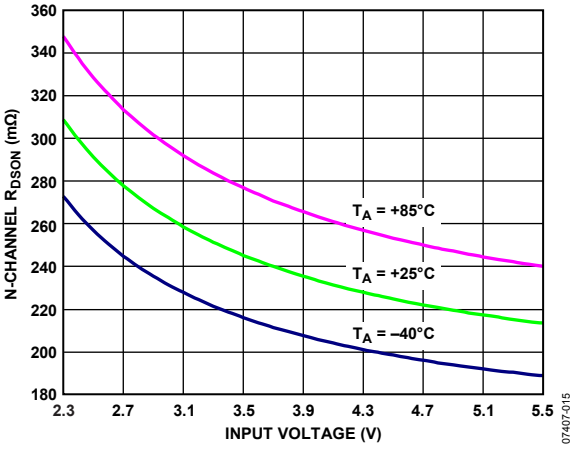

Figure 15. N-Channel Drain-Source On Resistance

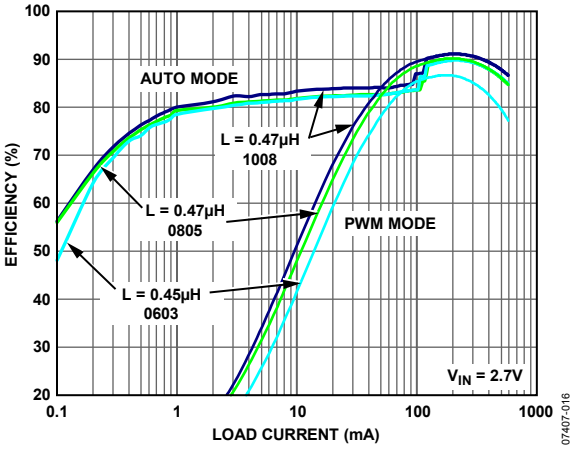

Figure 16. Efficiency for Various Inductor Sizes

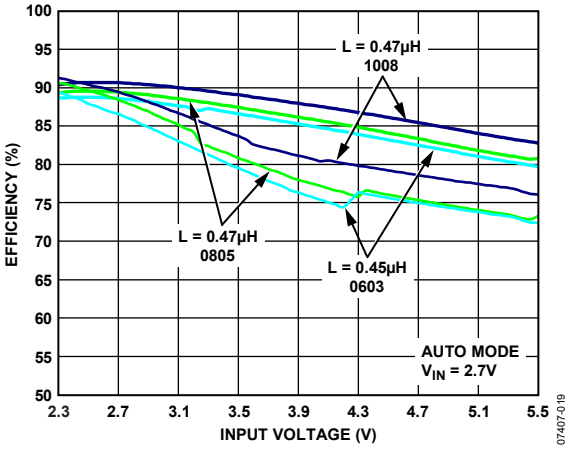

Figure 19. Efficiency vs. Input Voltage for Various Inductor Sizes

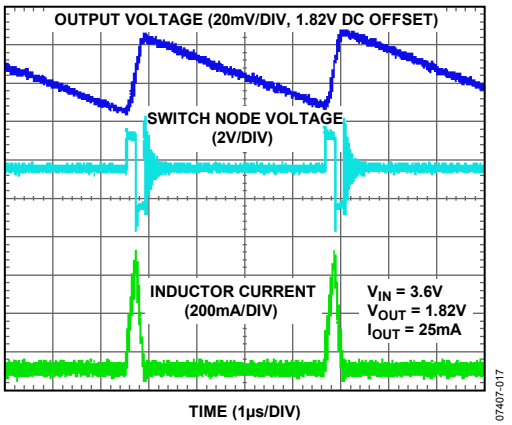

Figure 17. PFM Mode Operation

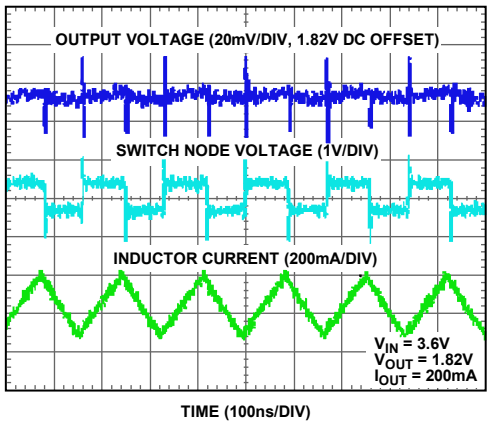

Figure 20. PWM Mode Operation

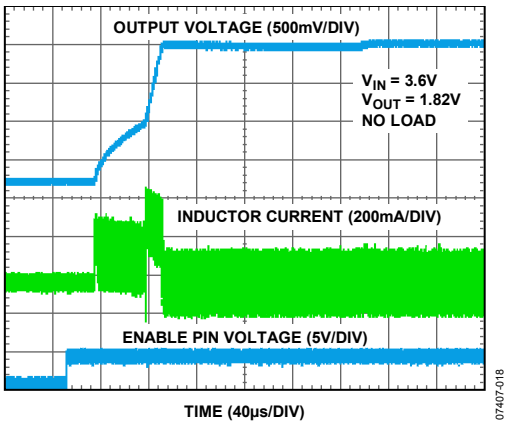

Figure 18. Start-Up Waveform, No Load

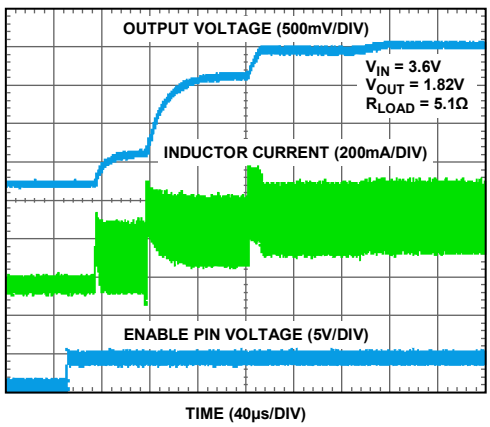

Figure 21. Start-Up Waveform, Heavy Load

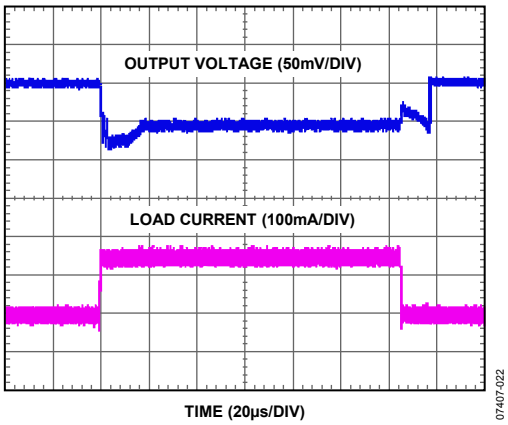

Figure 22. Load Transient Response, 0 mA to 150 mA (V_{IN} = 2.5 V, Auto Mode)

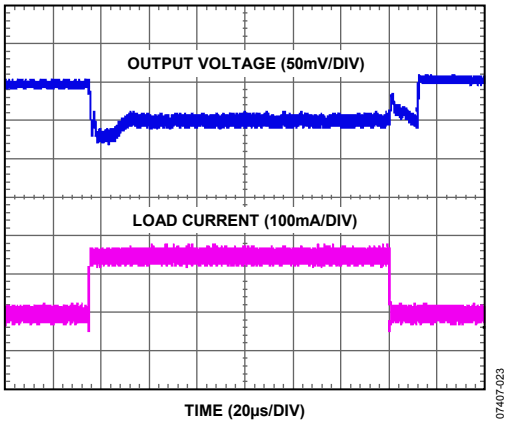

Figure 23. Load Transient Response, 0 mA to 150 mA (V_{IN} = 3.6 V, Auto Mode)

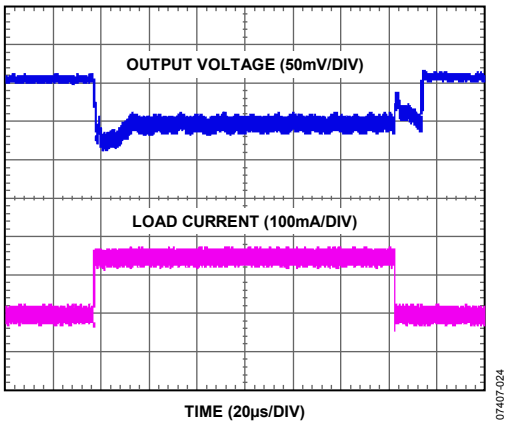

Figure 24. Load Transient Response, 0 mA to 150 mA (V_{IN} = 4.5 V, Auto Mode)

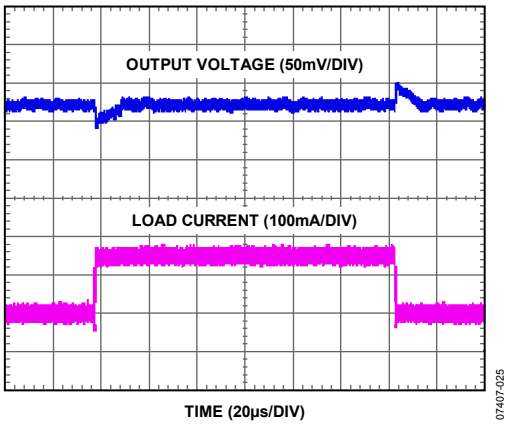

Figure 25. Load Transient Response, 0 mA to 150 mA (V_{IN} = 2.5 V, PWM Mode)

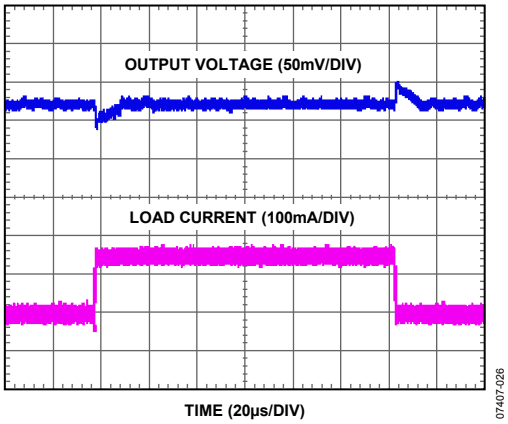

Figure 26. Load Transient Response, 0 mA to 150 mA (V_{IN} = 3.6 V, PWM Mode)

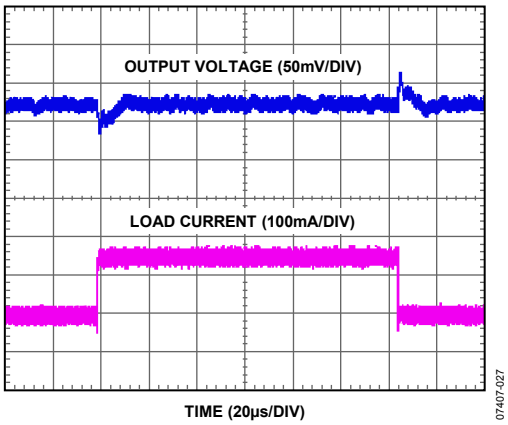

Figure 27. Load Transient Response, 0 mA to 150 mA (V_{IN} = 4.5 V, PWM Mode)

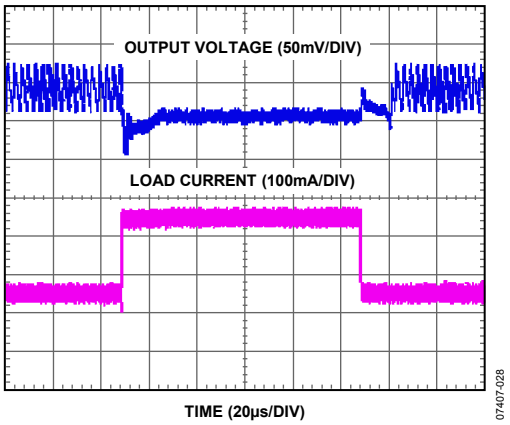

Figure 28. Load Transient Response, 50 mA to 250 mA (V_{IN} = 2.5 V, Auto Mode)

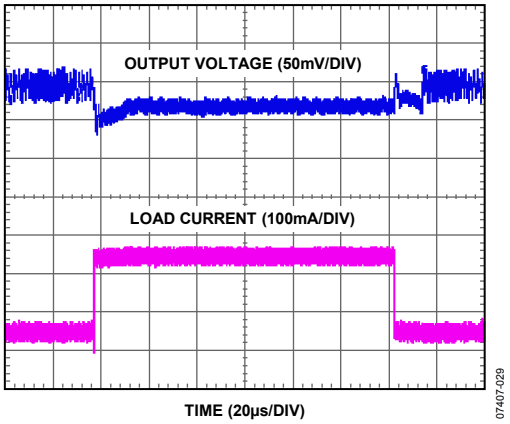

Figure 29. Load Transient Response, 50 mA to 250 mA (V_{IN} = 3.6 V Auto Mode)

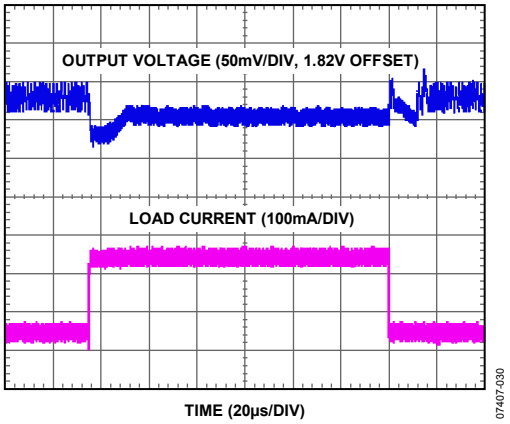

Figure 30. Load Transient Response, 50 mA to 250 mA (V_{IN} = 4.5 V, Auto Mode)

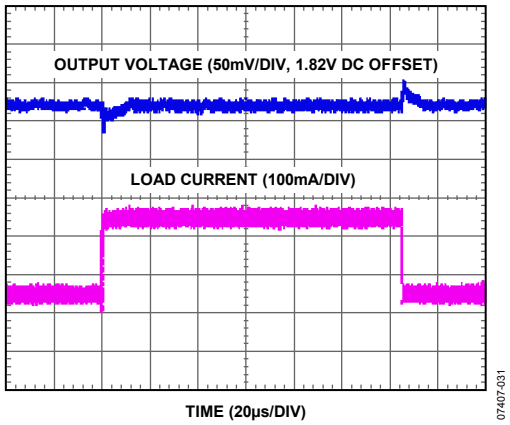

Figure 31. Load Transient Response, 50 mA to 250 mA (V_{IN} = 2.5 V, PWM Mode)

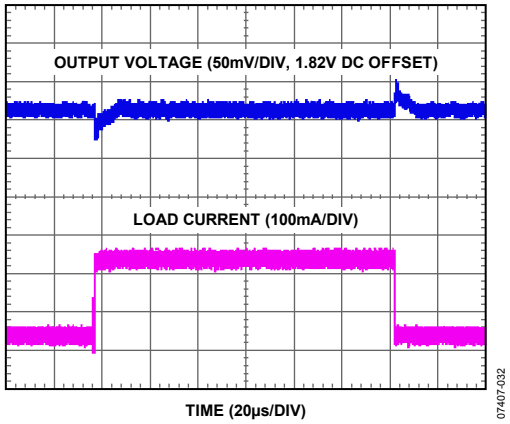

Figure 32. Load Transient Response, 50 mA to 250 mA (V_{IN} = 3.6 V, PWM Mode)

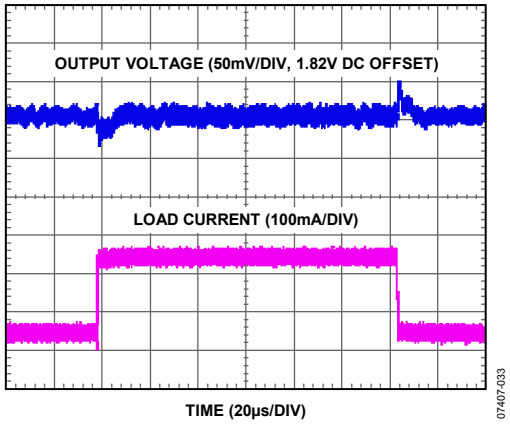

Figure 33. Load Transient Response, 50 mA to 250 mA (V_{IN} = 4.5 V, PWM Mode)

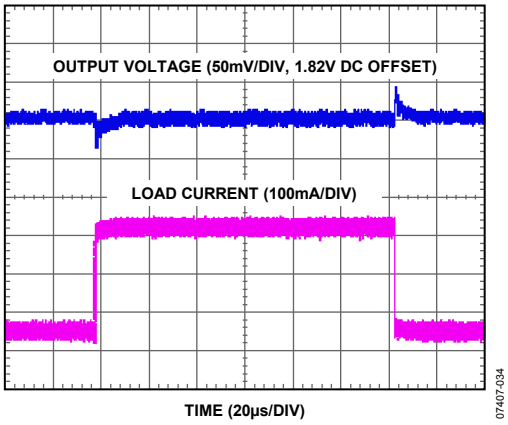

Figure 34. Load Transient Response, 150 mA to 400 mA (V_{IN} = 2.5 V, PWM Mode)

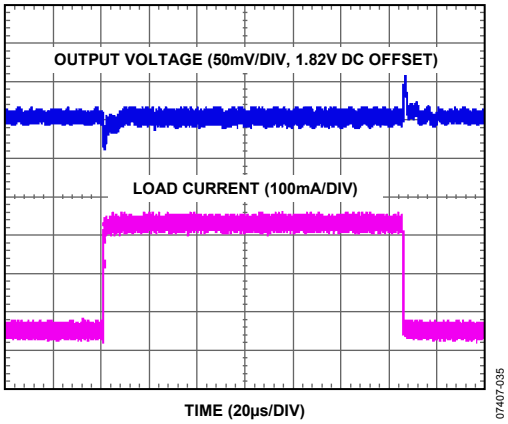

Figure 35. Load Transient Response,150 mA to 400 mA (V_{IN} = 3.6 V, PWM Mode)

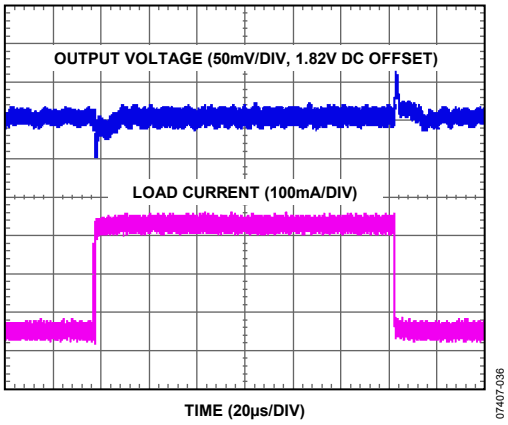

Figure 36. Load Transient Response, 150 mA to 400 mA (V_{IN} = 4.5 V, PWM Mode)

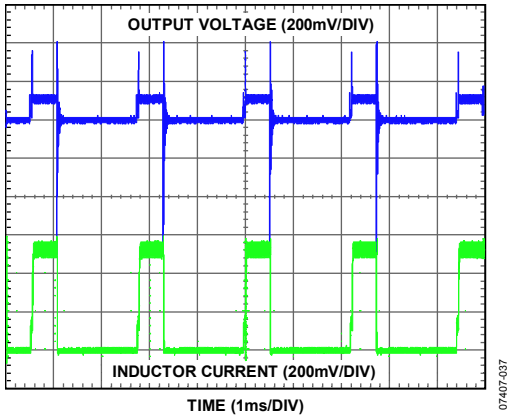

Figure 37. Output Short Circuit Response

THEORY OF OPERATION

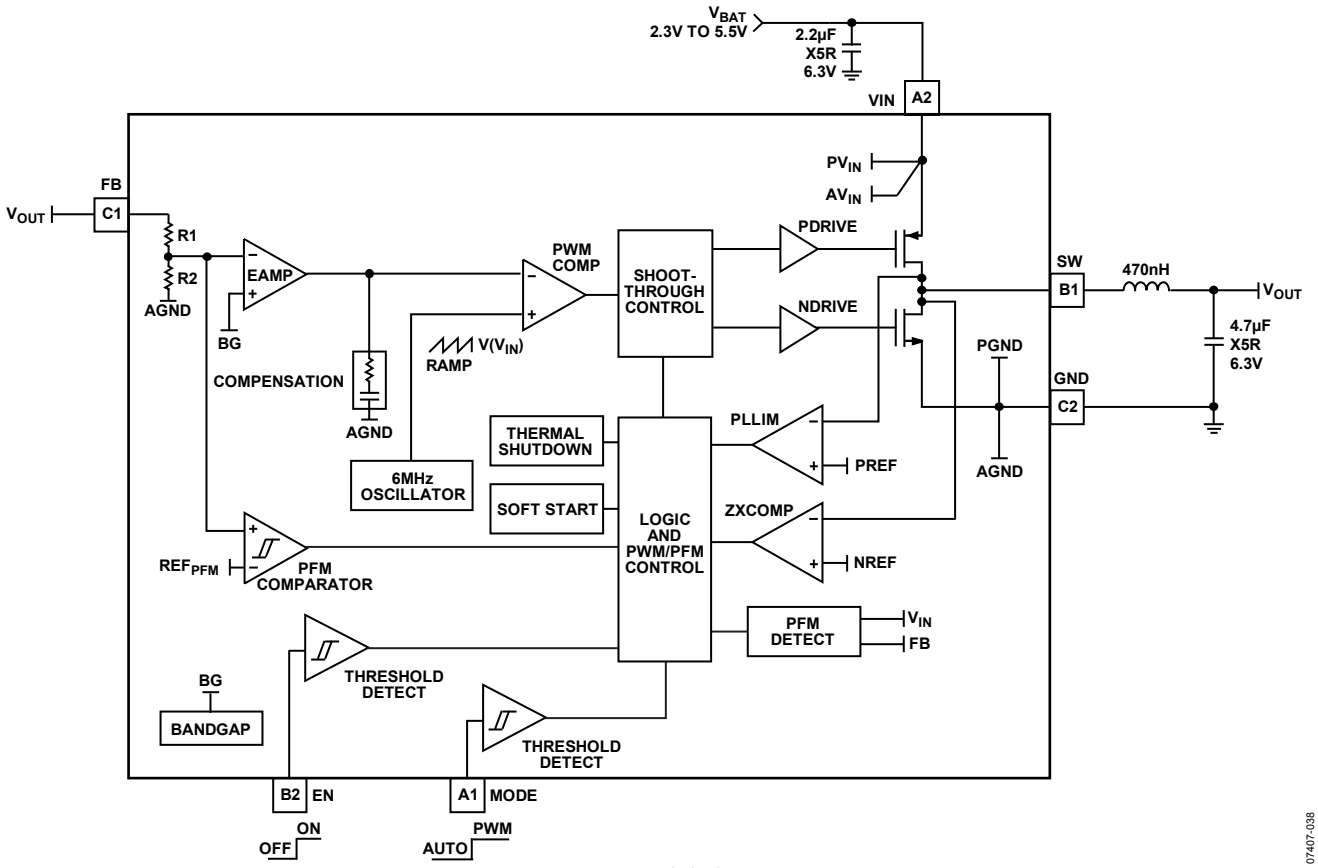

Figure 38. Internal Block Diagram

OVERVIEW

The ADP2121 is a high efficiency, synchronous, step-down, dc-to-dc converter that operates from a 2.3 V to 5.5 V input voltage. It provides up to 600 mA of continuous output current at a fixed 1.82 V (typical) output voltage. The 6 MHz operating frequency enables the use of tiny external components. The internal control schemes of the ADP2121 give excellent stability and transient response. External control for mode selection and device enable provide power-saving options that are aided by internal features such as synchronous rectification and compensation. Other internal features such as cycle-by-cycle peak current limit, soft start, undervoltage lockout, output-to-ground short circuit protection, and thermal shutdown provide protection for internal and external circuit components.

MODE SELECTION

The ADP2121 has two modes of operation, determined by the state of the MODE pin: PWM and auto.

Pull the MODE pin high to force the converter to operate in PWM mode regardless of the output current. Otherwise, set MODE low to allow the converter to automatically enter the power saving PFM mode at light load currents. Do not leave this pin floating. The MODE pin is not designed for dynamic control and should not be changed after the ADP2121 is enabled.

Pulse-Width Modulation (PWM) Mode

The PWM mode forces the part to maintain a fixed frequency of 6 MHz (typical) over all load conditions. The ADP2121 uses a hybrid proprietary voltage mode control scheme to control the duty cycle over load current and line voltage variation. This control provides excellent stability, transient response, and output regulation but results in lower efficiencies at light load currents.

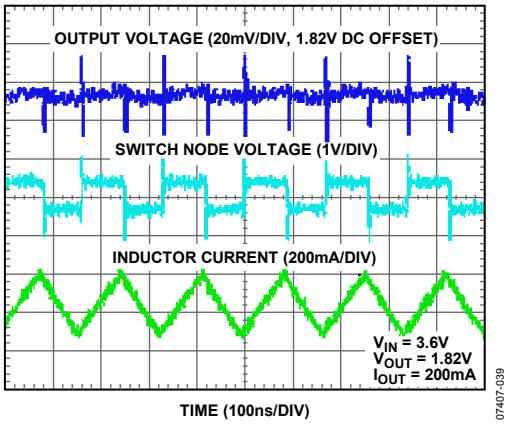

Figure 39. Typical PWM Operation

Auto Mode (PFM and PWM Switching)

Auto mode is a power saving feature that enables the converter to switch between PWM and PFM in response to the output load. Auto mode is enabled when the mode pin is pulled low. In auto mode, the ADP2121 operates in PFM mode for light load currents and switches to PWM mode for medium and heavy load currents (see Figure 40).

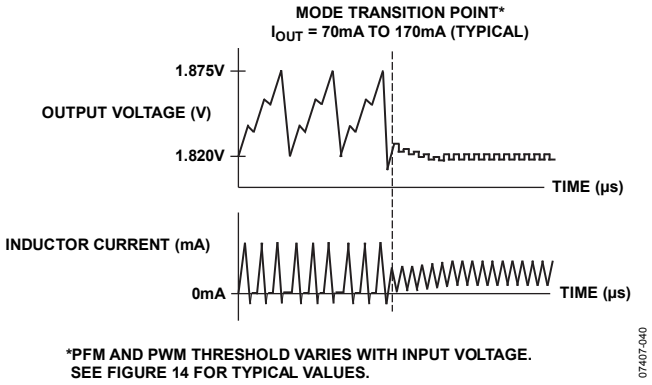

Figure 40. PFM-to-PWM Transition Point

Pulse Frequency Modulation (PFM)

When the converter is operating under light load conditions, the effective switching frequency and supply current are decreased and varied using PFM to regulate the output voltage. This results in improved efficiencies and lower quiescent currents. In PFM mode, the converter only switches when necessary to keep the output voltage within the PFM limits set by an internal comparator (see Figure 40). Switching stops when the upper limit is reached and resumes when the lower limit is reached.

Once the upper level is reached, the output stage and oscillator turn off to reduce the quiescent current. During this stage, the output capacitor supplies the current to the load. As the output capacitor discharges and the output voltage reaches the lower PFM comparator threshold, switching resumes and the process repeats. The output voltage, switching node voltage, and inductor current during this process are shown in Figure 41.

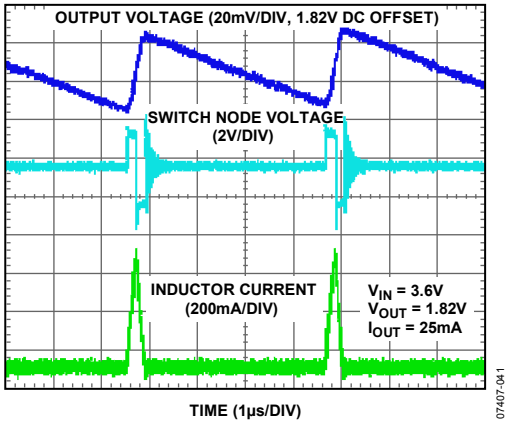

Figure 41. Typical PFM Operation

Mode Transition

When the mode pin is low, the converter switches between PFM and PWM modes automatically to maintain optimal transient response and efficiency. The mode transition point depends on input voltage. Hysteresis exists in the transition point to prevent instability and decreased efficiencies that could result if the converter were able to oscillate between PFM and PWM for a fixed input voltage and load current. See Figure 14 for typical values.

A switch from PFM to PWM occurs when the output voltage dips below the 1.82 V PWM output voltage level. Switching to PWM allows the converter to maintain efficiency and supply a larger current to the load.

The switch from PWM to PFM occurs when the output current is below the PFM threshold for multiple consecutive switching cycles. Switching to PFM allows the converter to save power by supplying the lighter load current with fewer switching cycles.

Figure 40 shows that the output voltage in PFM mode is slightly higher to keep ADP2121 from oscillating between modes and ensure stable operation.

ENABLE/SHUTDOWN

The EN input turns the ADP2121 on or off. Connect EN to GND or logic low to shut down the part and reduce the current consumption to 0.3 µA (typical). Connect EN to VIN or logic high to enable the part. Do not leave this pin floating.

INTERNAL CONTROL FEATURES

Overcurrent Protection

To ensure that excessively high currents do not damage the inductor, the ADP2121 incorporates cycle-by-cycle overcurrent protection. This function is accomplished by monitoring the instantaneous peak current on the power PMOS switch. If this current exceeds the maximum level (1 A typical), then the PMOS is immediately turned off. This minimizes the potential for damage to power components during certain faults and transient events. The value listed in Table 1 is an open loop dc tested value. Inherent delays in the current limit comparator allow a slight increase and variation in this specification.

Soft Start

To prevent excessive input inrush current at startup, the ADP2121 operates with an internal soft start. When EN goes high, or when the part recovers from a fault (UVLO, TSD, or short-circuit protection), a soft start timer begins. The soft start timer corresponds to the maximum soft start period for the given fixed output voltage. During this time, the peak current limit is gradually increased to its maximum. As seen in Figure 18 and Figure 21, the output voltage passes through several stages to ensure that the converter is able to start up effectively and in proper sequence. After the soft start period has expired, the peak current limit remains at 1 A (typical), and the part enters the operating mode determined by the MODE pin.

Synchronous Rectification

In addition to the P-channel MOSFET switch, the ADP2121 includes an N-channel MOSFET switch to build the synchronous rectifier. The synchronous rectifier improves efficiency, especially for small load currents, and reduces cost and board space by eliminating the need for an external rectifier.

Compensation

The control loop is internally compensated to deliver maximum performance with no additional external components. The ADP2121 has been designed to work with 0.47 µH chip inductors and 4.7 µF capacitors (see Table 5, Table 6, and Table 7.) Other values may reduce performance and/or stability.

Undervoltage Lockout (UVLO)

If the input voltage is below the UVLO threshold, the ADP2121 automatically turns off the power switches and places the part into a low power consumption mode. This prevents potentially erratic operation at low input voltages. The UVLO levels have approximately 100 mV of hysteresis to ensure glitch-free startup.

Output Short Circuit Protection

If the output voltage is inadvertently shorted to GND, a standard dc-to-dc controller delivers maximum power into that short. This could result in a potentially catastrophic failure. To prevent this, the ADP2121 senses when the output voltage is below the short circuit protection threshold (typically 1.24 V). At this point, the controller turns off for approximately 1.8 ms and then automatically initiates a soft start sequence. This cycle repeats until the short is removed or the part is disabled. This dramatically reduces the power delivered into the short circuit, yet still allows the converter to recover if the fault is removed.

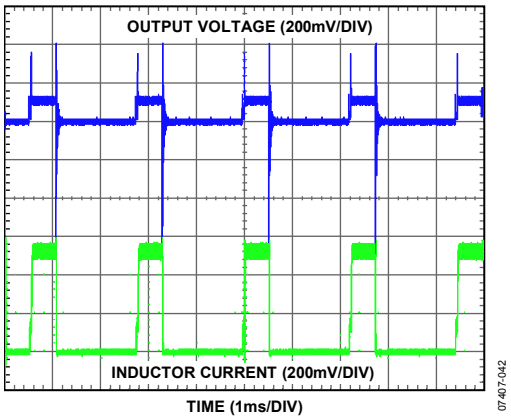

Figure 42. Output Short Circuit Protection, V_{OUT} = 1.82 V

Thermal Shutdown (TSD) Protection

The ADP2121 also includes TSD protection. If the die temperature exceeds 150°C (typical), the TSD protection activates and turns off the power devices. They remain off until the die temperature falls below 135°C (typical), at which point the converter restarts.

APPLICATIONS INFORMATION

The external component selection for the ADP2121 applications circuit is driven by the load requirement and begins with the selection of the inductor. After the inductor is chosen, C_{IN} and C_{OUT} can be selected. Components can be identified using the selection guide and recommended selection tables in this section.

INDUCTOR SELECTION

The high switching frequency of the ADP2121 allows for minimal output voltage ripple, even with small inductors. Inductor sizing is a trade-off between efficiency and transient response. A small inductor leads to a larger inductor current ripple that provides better transient response but degrades efficiency. Due to the high switching frequency of the ADP2121, multilayer ceramic inductors can be used for an overall smaller solution size. Shielded ferrite core inductors are recommended for their low core losses and low electromagnetic interference (EMI).

As a guideline, the inductor peak-to-peak current ripple is typically set to

$$\Delta I_L = 0.45 \times I_{LOAD} \quad (1)$$

where I_{LOAD} is the maximum output current. The largest ripple current, ΔI_L, occurs at the maximum input voltage.

It is important that the inductor be capable of handling the maximum peak inductor current, I_{PK}, determined by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \Delta I_L/2 \quad (2)$$

The dc current rating of the inductor should be greater than the calculated I_{PK} to prevent core saturation. The ADP2121 is designed for applications with a 0.47 µH inductor. Other values are not recommended; and stable operation over all conditions is not guaranteed with their use. Table 5 shows the available 0.47 µH surface mount inductors that have been tested with the ADP2121.

INPUT CAPACITOR SELECTION

The input capacitor must be able to support the maximum input operating voltage and the maximum rms input current. Select an input capacitor capable of withstanding the rms input current for the maximum load current in the application using the following equation:

$$I_{rms} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (3)$$

The input capacitor reduces the input voltage ripple caused by the switch currents on the VIN pin. Place the input capacitor as close as possible to the VIN pin.

In principle, different types of capacitors can be considered, but for battery-powered applications, the best choice is the multilayer ceramic capacitor, due to its small size and low equivalent series resistance (ESR). Table 6 offers input capacitor suggestions. All capacitors listed in the table are multilayer ceramic capacitors.

It is recommended that the VIN pin be bypassed with a 2.2 µF or larger ceramic input capacitor if the supply line has a distributed capacitance of at least 10 µF. If not, then at least a 10 µF capacitor is recommended on the input supply pin. The input capacitor can be increased without any limit for better input voltage filtering. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5U and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. For a given loop crossover frequency (the frequency at which the loop gain drops to 0 dB), the maximum voltage transient excursion (overshoot) is inversely proportional to the value of the output capacitor. The ADP2121 has been designed to operate with small ceramic capacitors in the 4.7 µF to 10 µF range that have low ESR and equivalent series inductance (ESL). These components are able, therefore, to meet tight output voltage ripple specifications. X5R or X7R dielectrics with a voltage rating of 6.3 V are recommended. Table 7 shows a list of output MLCC capacitors recommended for ADP2121 applications. The minimum effective capacitance required for stable operation is 1.5 µF.

When choosing output capacitors, it is also important to account for the loss of capacitance due to output voltage dc bias. This can result in using a capacitor with a higher rated voltage to achieve the desired capacitance value. Additionally, if ceramic output capacitors are used, the capacitor rms ripple current rating should always meet the application requirements. The rms ripple current is calculated as

$$I_{rms(COUT)} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{L \times f_{SW} \times V_{IN(MAX)}} \quad (4)$$

At nominal load currents, the converter operates in forced frequency mode (PWM), and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor.

$$\Delta V_{OUT} = \Delta I_L \times (ESR + 1/(8 \times C_{OUT} \times f_{SW})) \quad (5)$$

The largest voltage ripple occurs at the highest input voltage. At light load currents, if MODE is set low, then the converter operates in power save mode (PFM), and the output voltage ripple increases.

Table 5. Recommended Inductor Selection

Manufacturer	Series	Inductance (µH)	DCR (mΩ)	Current Rating (mA)	Size (L × W × H) (mm)	Package
Murata	LQM2HPNR47MG0L	0.47 ± 20%	40 ± 25%	1800	2.50 × 2.00 × 0.90	1008
	LQM21PNR47MC0D	0.47 ± 20%	120 ± 25%	1100	2.00 × 1.25 × 0.50	0805
Taiyo Yuden	BRC1608TR45M	0.45 ± 20%	117 ± 30%	800	1.60 × 0.80 × 0.80	0603
TDK	MLZ2012DR47MT	0.47 ± 20%	180 ± 30%	550	2.00 × 1.25 × 1.25	0805
	GLFR1608TR47M-LR	0.47 ± 20%	50 ± 30%	1100	1.36 × 0.80 × 0.80	0603

Table 6. Recommended Input Capacitor Selection

Manufacturer	Part Number	Capacitance (µF)	Voltage Rating (V)	Temperature Coefficient	Size (L × W × H) (mm)	Package
Murata	GRM155R60J225M	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402
Taiyo Yuden	JMK105BJ225MV-F	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402
Panasonic	ECJ-0EB0J225M	2.2	6.3	X5R	1.0 × 0.5 × 0.5	0402

Table 7. Recommended Output Capacitor Selection

Manufacturer	Part Number	Capacitance (µF)	Voltage Rating (V)	Temperature Coefficient	Size (L × W × H) (mm)	Package
Murata	GRM188R60J475KE19D	4.7	6.3	X5R	1.6 × 0.8 × 0.8	0603
	GRM155R60J475ME87D	4.7	6.3	X5R	1.0 × 0.5 × 0.5	0402
Taiyo Yuden	AMK105BJ475MV-F	4.7	4	X5R	1.0 × 0.5 × 0.5	0402
Panasonic	ECJ-0EB0J475M	4.7	6.3	X5R	1.0 × 0.5 × 0.5	0402

PCB LAYOUT GUIDELINES

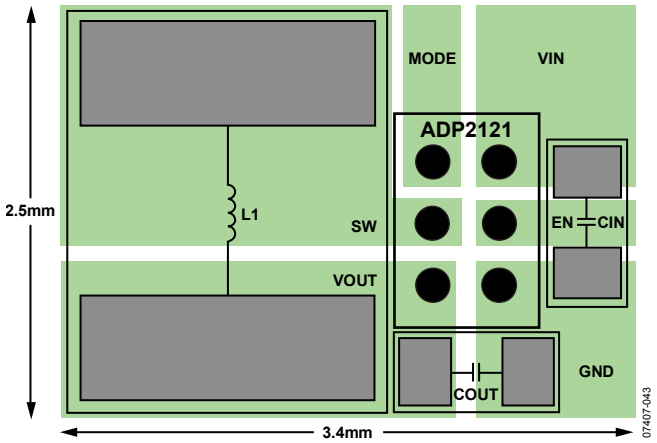

Figure 43. Solution Size with a 1008 Inductor

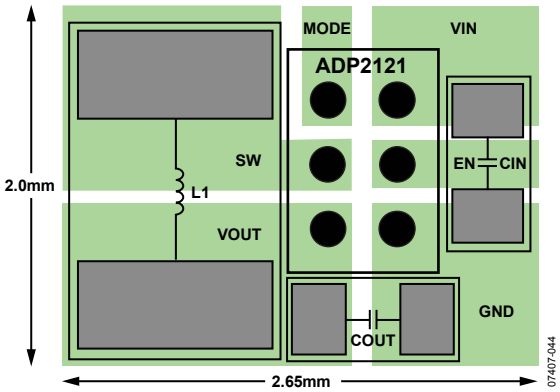

Figure 44. Solution Size with a 0805 Inductor

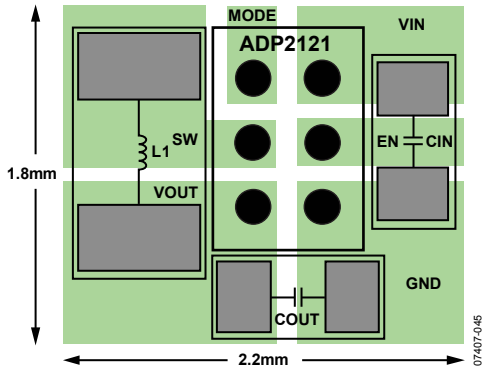

Figure 45. Solution Size with a 0603 Inductor

For high efficiency, good regulation, and stability with the ADP2121, a well-designed PCB is required.

Use the following guidelines when designing PCBs:

- Keep the low ESR input capacitor, CIN, close to VIN and GND.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, COUT, close to FB and GND of the ADP2121. Long trace lengths from the part to the output capacitor add series inductance that may cause instability or increased ripple.

OUTLINE DIMENSIONS

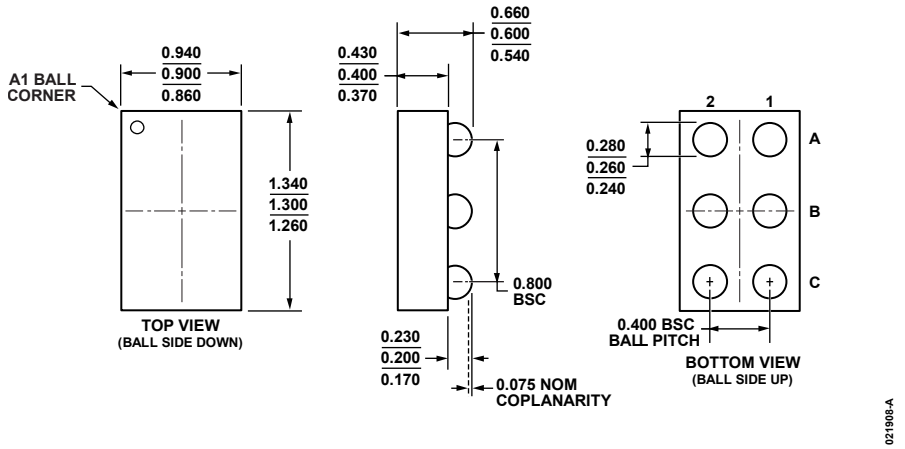

Figure 46. 6-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-6-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP2121ACBZ-1.82R7[1, 2]	−40 °C to +85 °C	1.82	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-4	L7N
ADP2121-1.82-EVALZ[1]		1.82	Evaluation Board for 1.82 V		

[1] Z = RoHS Compliant Part.
[2] Halide free.

NOTES

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